Description

Method for synchronizing a plurality of digital input signals

The invention relates to a method for synchronizing a plurality of digital input signals which are formed by sampling with the aid of a dedicated operating clock in each case.

A method of this type can be gathered from the European patent specification EP 0 198 684 B1. According to this method, specifically, a differential relay described in this patent specification operates to protect an electric power transmission line which is monitored at various points with regard to the current flowing through. The currents at the various points on the power transmission line are converted into digital input signals by using a dedicated operating clock in each case to sample the power supply line to be monitored at the various points; the sampling is undertaken in this case at the various points not with the aid of a synchronous clock, but with the aid of weakly differing clock frequencies. Running between the various points of the power supply line is a digital transmission channel via which a calling message is transmitted by a detecting device (master) at one point of the power supply line to another point, the calling message also including data which give information on the sampling instant at the one point. In response to the calling message, a detecting device (slave) at the other point of the power supply line emits a return signal which includes, inter alia, the information on the sampling instant in the master and on a time difference between the last sampling instant in the slave

and the subsequent receiving instant of the calling message in the slave. The return signal received by the master is used in the master to draw a conclusion on the temporal skew of the sampling instants at the two different points on the power supply line, and the time skew is compensated with regard to the various sampling instants after a vector transformation of the received data by means of an appropriate pointer rotation.

It is the object of the invention to develop a method for synchronizing a plurality of digital input signals such that it can be carried out relatively easily and reliably without the need to form pointer variables.

According to the invention, in order to achieve this object in the case of a method of the type specified at the beginning, digital auxiliary signals are formed by sampling the digital input signals with the aid of a common postprocessing clock, use being made of a postprocessing clock which is at least twice as fast as the slowest operating clock; synchronized digital output signals which correspond to the digital input signals are formed by means of interpolating each digital auxiliary signal.

A substantial advantage of the method according to the invention consists in that it can be used to synchronize a plurality of digital input signals even when these input signals are formed from analog input signals by sampling with the aid in each case of a very different operating clock. Consequently, the clock generators required for generating the operating clocks need to fulfil only relatively low requirements for the purpose of carrying out the method according to the invention. Moreover,

the method according to the invention places relatively modest requirements on the quality of the transmission channels. A further important advantage consists in that the method according to the invention can be carried out relatively easily, because the sampling of digital input signals with the aid of a common postprocessing clock, and the interpolation of the digital auxiliary variables thus formed are well-established measures per se.

The method according to the invention can be carried out with sufficient accuracy whenever the digital input variables are sinusoidal and/or cosinusoidal signals. This is frequently not the case, and so it is necessary then to accept relatively large errors. If this is not acceptable with regard to the given requirements, it seems to be advantageous in accordance with a development of the invention when, before being sampled with the aid of the common postprocessing clock, the digital input signals are filtered with the aid of a filter having a characteristic which is the inverse of the characteristic of an interpolation filter used for the interpolation. In this embodiment of the method according to the invention, a transmission characteristic with the value 1 results on the transmission link of the digital input variables up to the formation of the digital output variables, resulting in the possibility of forming digital output variables which correspond very perfectly to the digital input variables.

It has proved to be advantageous in the case of the method according to the invention when filtering with the aid of an antialiasing filter is undertaken directly after the interpolation, in order to achieve a bandwidth limitation for an evaluation device to which the digital output signals are to be applied.

The digital input signals to be synchronized can be of very different formation. For example, they can be output signals of sensors which respectively use individual clock generators to output digital signals at their output from analog input variables. Furthermore, the digital input signals can be generated from analog measured variables of an electric power supply system by sampling at various points on the power supply system. The method according to the invention is to be regarded as particularly advantageous when the digital input variables are obtained from secondary variables, sampled with the aid in each case of a dedicated operating clock, of measuring transducers in an electric power supply system. In this case, the measuring transducers can be arranged at various positions, for example in a transformer substation, or can be obtained as a component of a differential protective arrangement at the ends of an electric power supply line or at other terminals of a generator or power transformer.

If the measuring transducers are Rogovsky measuring transducers, the digital input signals formed from the secondary variables of such measuring transducers are converted directly into the digital auxiliary variables, and an integrator is used for the interpolation.

For the purpose of further explaining the invention, Figure 1 illustrates an exemplary embodiment of an arrangement for carrying out the method according to the invention, in the form of a block diagram,
Figure 2 shows an exemplary embodiment of a filter for filtering the digital input variables,
Figure 3 shows the characteristic and structure of the filter according to Figure 2,

Figure 4 illustrates an exemplary embodiment of an interpolation filter, and

Figure 5 shows the characteristic and structure of the filter according to Figure 4.

As may be seen from Figure 1, there is present at an input 1 of an arrangement for carrying out the method according to the invention an analog input signal x(t) which is converted in an analog-to-digital converter 2 into a digital input signal x(k). This digital input signal x(k) traverses a signal encoder 3 formed by a differentiator, resulting at the output of the signal encoder 3 in a pulse train xd(k) which has been produced by differentiating the digital input signal x(k). A transmission device 4 transmits the pulse train xd(k) via a transmission channel 5 to a receiving device 6 which outputs the pulse train xd(k) on the output side.

The arrangement illustrated in Figure 1 includes a further receiving device 7 which is connected with its input 8 to a further input 9 of the arrangement in a way which was described in conjunction with the receiving device 6 with reference to the input 8. The dotted illustration is intended to include an analog-to-digital converter corresponding to the analog-to-digital converter 2, a signal encoder corresponding to the signal encoder 3, a transmitting device corresponding to the transmitting device 4, and a transmission channel corresponding to the transmission channel 5. A pulse train yd(k) obtained in accordance with the pulse train xd(k) of the signal y(t) is then produced at the output of the further receiving device 7.

In addition to the receiving device 7, it is also possible for further additional receiving devices to have additional pulse trains applied to them in the same way.

On the output side, a signal decoder 10, which includes a resampling device 11 on the input side, is connected to the receiving devices 6 and 7. This resampling device 11 can be designed and operated as illustrated in detail in US patent 5,075,880, particularly in Figure 5, and described in conjunction therewith. Thus, in the resampling device 11 the digital input signals xd(k) and yd(k) are respectively sampled per se with the aid of a common postprocessing clock of the resampling device, and digital auxiliary signals xd(nk+j) and yd(nk+j) are formed in the process by the insertion of zero values. In this case, the resampling device 11 is designed with regard to its postprocessing clock such that the latter is at least twice as fast as the fastest operating clock during the formation of the digital input signals x(k). For example, if the sampling frequencies for obtaining the digital input signals x(k) are between approximately 1 and 40 kHz, a frequency range of between 10 and 500 kHz comes into consideration for the postprocessing clock; approximately 200 kHz may be recommended.

The digital auxiliary signals xd(nk+j) and yd(nk+j) with the comparatively high postprocessing clock are fed in each case to an interpolation filter 12 and 13, respectively, which is an integrator in each case in the exemplary embodiment illustrated. The integrators are used in each case because differentiators have been used as signal encoders 3. A transmission characteristic with the value 1 thereby results with regard to the mode of operation of the signal encoder 3 and of the integrator 12 of the signal decoder 10.

Other interpolation filters also basically come into consideration, for example Lagrange interpolators or Spline interpolators.

The pulse trains x(nk+j) and y(nk+j) formed at the output of the integrators 12 and 13 are synchronized and are respectively fed to an antialiasing filter 14 and 15, by means of which filters the pulse trains are limited to the bandwidth required for processing in an evaluation device (not illustrated). The result is the reduction of digital output signals x(m) at the output of one antialiasing filter 14, and y(m) at the output of the other antialiasing filter 15. These digital output signals x(m) and y(m) can now be reduced in a known way to a sampling rate which is suitable for an evaluation device (not illustrated). This sampling rate must be produced by means of an integral devisor from the sampling rate of the resampling device 11. For the assumed frequencies, reasonable values here are between 0.6 and 10 kHz for applications in the monitoring of electric power supply systems.

If x(t) and y(t) are pure sinusoidal or cosinusoidal signals, it is then possible to dispense with the signal encoder 3 in each case. This also holds in the case of signals which are not pure sinusoidal or cosinusoidal ones whenever x(t) and y(t) are output variables of Rogovsky transducers because these output variables correspond to the differential quotient of the transducer input variables.

Illustrated in Figure 2 is an exemplary embodiment for a signal encoder 3 in accordance with Figure 1, which is designed as an FIR filter acting as a differentiator. Here, A denotes the input of the signal encoder, and B denotes the output. The digital input signal x(k) is used to form

the pulse train xd(k). The coefficients a_0, a_1 and b_1 of the signal coder 3 are dimensioned as follows:

Coefficient	Value
a0	0.66666666666667
a1	-0.66666666666667
b1	0.83333333333333

In the top illustration of Figure 3, the amplitude characteristic is illustrated plotted against the frequency of the signal encoder according to Figure 2, while in the bottom illustration of Figure 3 the phase characteristic is reproduced plotted against the frequency of such a filter.

The interpolation device 12 illustrated in Figure 4, or the interpolation device 13 in accordance with Figure 1 shows an FIR filter as integrator having coefficients a_0, a_1, b_1 dimensioned in a way which may be gathered from the following table. C denotes the input of this FIR filter, and D denotes its output.

Coefficient	Value
a0	1.50000000000000
a1	1.25000000000000
b1	-1

In the top illustration of Figure 5, the amplitude characteristic is shown plotted against the frequency of the filter according to Figure 4, and in the bottom illustration of Figure 5 the phase characteristic is shown plotted against the frequency of such a filter. It may be seen that the frequency characteristics of the filters according to Figures 2 and 4 are inverse relative to one another, and this leads to the targeted transmission function having the value 1.